CLEAN SETS OF CLAIMS

We claim:

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1. An active electronic isolator between a source stage and a load stage, including at least one circuit path into which electrical noise is directed away from said source and said load stages, including configuring means for configuring said path to appear as an infinite impedance to the output signal from said source stage.

2. The electronic isolator of claim 1 wherein said configuring means comprises a voltage source.

3. The electronic isolator of claim 2 wherein said isolator comprises a T-configuration coupled to said voltage source.

4. The electronic isolator of claim 3 wherein said voltage source is a controllable voltage source.

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13. An active electronic isolator between a source stage and a load stage comprising:

an electrical input comprising at least one source electrical connection connected to the source stage,

an electrical output comprising at least one load electrical connection to the load stage,

at least one circuit path into which electrical noise is directed away from the source and load electrical connections,

in which insertion loss of said electronic isolator is dependent upon the direction of signal and noise transmission through said electronic isolator.

14. The electronic isolator of claim 13 wherein insertion loss from the electrical input to the electrical output is substantially less than insertion loss from the electrical output to the electrical input.

16. The electronic isolator of claim 13 wherein at least one of said electrical input and said electrical output comprise at least one conductor using a ground signal return path.

21. The electronic isolator of claim 13 including a controllable source that is a current or voltage controlled voltage source circuit.

57. The electronic isolator of claim 21 wherein said controllable source is a pulsed voltage source.

69. The electronic isolator of claim 4 wherein said controllable voltage source adds or removes signal at the common node within said T-configuration such that substantially all of the source signal current is conducted to the load stage, and all other currents interring the node are directed into the circuit path within the T-configuration that is not connected to the source stage or load stage.